IK GUJRAL PUNJAB TECHNICAL UNIVERSITY

Scheme and Syllabus
of
Master of Technology
(VLSI Design)

Batch 2016
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<th>Semester-I</th>
<th>Course Code</th>
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S-Satisfactory, US-Unsatisfactory
Elective-I
MTVL-205  Advanced Digital Signal Processing
MTVL-206  Semiconductor Devices
MTVL-207  VLSI Interconnects

Elective-II
MTVL-208  Memory Design and Testing
MTVL-209  Low Power VLSI Design
MTVL-210  Modeling and Simulation

Elective-III
MTVL-304  System on Chip (SOC)
MTVL-305  RF Circuit Design
MTVL-306  Advanced Computer Architecture
MTVL-307  Process and Device Characterization & Measurements

Elective-IV
MTVL-308  Sensor Technology and MEMS
MTVL-309  Nanoelectronics Devices
MTVL-310  Biomedical Electronics
MTVL-311  Hardware-Software Co-design
MTRM-101 Research Methodology

Internal Marks: 50
External Marks: 100
Total Marks: 150

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Methods of Research: Nature and Objectives of research; historical, descriptive and experimental. Study and formulation of research problem. Scope of research and formulation of hypotheses; Feasibility, preparation and presentation of research proposal.

Introduction to Statistical Analysis: Measures of central tendency and dispersion: mean, median, mode, range, mean deviation and standard deviation. Regression and correlation analysis. Probability and probability distributions; Binomial, Poisson, Geometric, Negative binomial, Uniform, Exponential, Normal and Log-normal distribution. Basic ideas of testing of hypotheses; Tests of significance based on normal, t and Chi-square distributions. Analysis of variance technique.

Design of Experiments: Basic principles, study of completely randomized and randomized block designs. Edition and tabulation of results, presentation of results using figures, tables and text, quoting of references and preparing bibliography. Use of common softwares like SPSS, Mini Tab and/or Mat Lab. For statistical analysis.

Text Books / References

MTVL-102 VLSI Design concepts

Internal Marks: 50
External Marks: 100
Total Marks: 150

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**Introduction To MOS Circuits:** MOS Transistor Theory - Introduction MOS Device Design Equations, MOS Transistor as a Switches, Pass Transistor, CMOS Transmission Gate, Complementary CMOS Inverter, Static Load MOS Inverters, Inverters with NMOS loads, Differential Inverter, Tri State Inverter, BiCMOS Inverter.

**Circuit Characterization And Performance Estimation:** Delay Estimation, Logical Effort and Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, Design Margin and Reliability.

**CMOS Circuit And Logic Design:** CMOS Logic Gate Design, Physical Design of CMOS Gate, Designing with Transmission Gates, CMOS Logic Structures, Clocking Strategies, I/O Structures.

**CMOS Sub System Design:** Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multipliers, Shifters, Memory Elements, Control- FSM, Control Logic Implementation.


**Texts / References**

MTVL-103 Hardware Description Languages

Basic concepts of Hardware Description Languages: VLSI Design flow, Features of VHDL, Capabilities, Hierarchy, Syntax and Semantics of VHDL; Basic Language Elements- Data objects- Variable signal, and constant, Data types, Operators and signal assignments, Design Suits- Entities, architecture declaration, configurations, Packages.


Introduction to Verilog Hardware Description Language: Key features, Capabilities, Language Constructs and Conventions in Verilog, Syntax and Semantics of Verilog; Basic Language Elements: Operators, nets, registers, vectors, arrays, parameters, system tasks, compiler directives, Module, port connection rules.

Modeling Styles (Verilog): Gate Level Modeling- Gate types, Gate delays; Dataflow Modeling – continuous assignment, Behavioral Modeling- Initial & Always Construct, Assignments with Delays, wait construct, Multiple always blocks, If and if-else, assign, Loop Construct, Sequential and Parallel blocks, Switch level modeling- MOS switches, CMOS switches.

Design using VHDL/Verilog Unit- Combinational logics- Adder, Subtractor, Decoders, Encoders, Multiplexer, code Converter; Flip flop, state machines – Mealy type FSM, Moore type FSM, Counters and Shift register. Synthesis of digital logic circuits.

Text / References

MTVL-104 VLSI Technology

Internal Marks: 50  L    T    P
External Marks: 100
Total Marks: 150

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modeling and technology; Ion Implantation modeling, technology and damage annealing; characterization of Impurity profiles.

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation Technologies in VLSI and ULSI; Characterization of oxide films; High k and low k dielectrics for ULSI.

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.

Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal Interconnects; Multi-level metallization schemes.

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology

Text/References

4. VLSI Fabrication Technology, B. Raj & Singh, Laxmi Publications
7. A.S Grove, “Physics and Technology of semiconductor devices”, John Wiley & Sons
MTVL-105 Design of Analog/ Mixed Mode VLSI Circuits

Internal Marks:50
External Marks: 100
Total Marks:150

L T P
3 1 0

- Basic CMOS Circuit Techniques, Continuous Time And Low voltage Signal Processing: Mixed-Signal VLSI Chips, Analog MOSFET Modelling: MOS transistor, Low frequency MOSFET Models, High frequency MOSFET Models, Temperature effects in MOSFET, Noise in MOSFET.
- Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor- Primitive Analog Cells, Current Source, Sinks and References MOS Diode/Active resistor, Simple current sinks and mirror, Basic current mirrors, Advance current mirror, Current and Voltage references, Bandgap references.
- Sampled-Data Analog Filters, Over Sampled A/D Converters and Analog Integrated Sensors: First-order and Second SC Circuits-Bilinear Transformation – Cascade Design-Switched-Capacitor Ladder Filter

Text/References

3. CMOS: Circuit Design, Layout and Simulation by R. Jacob Baker, Harry W. Li, and David E. Boyce, Prentice Hall of India
4. Analog Integrated circuit Design by David A. Johns and Ken Martin, John Wiley & Son
5. Greogorian & Tames, “ Analog Integrated Circuit For Switched Capacitor Circuit “
MTVL-106 Lab – I

Internal Marks:100
External Marks: -
Total Marks:100

L T P
0 0 4

2 Bit-Counter: The purpose of this lab is to write a HDL description of 2-bit counter as a finite state machine. The 2-bit counter has several inputs such as clk, rst, enable, load, count-up or count-down etc.

Parallel to Serial Converter: The purpose of this lab is to write a HDL description of a parallel to serial converter as an FSMD. The parallel to serial converter will accept an eight-bit number and send one bit of data over the data line per clock cycle. There is also a go bit, which tells the converter to start transmitting data.

VHDL Calculator: The purpose of this lab is to implement a finite state machine in VHDL to perform simple calculations like addition, subtraction, and multiplication

A Simplified HDL UART: In this lab the students design a UART to send data to the PC.

I2C Bus: HDL implementation of I2C bus protocol

Design of a Hardware Multiplier: In this lab students are going to implement hardware multiplier using Sequential Circuit Components.

ALU Design: The purpose of this lab is to build a 4/8 -bit ALU. The ALU is written behaviorally. It should take in two numbers and be able to add the numbers, subtract the numbers, NOR the numbers, or NAND the numbers.

NMOS Inverter: Depletion and enhancement mode inverter circuit simulation and modification in circuit parameters.

CMOS Inverter: Circuit simulation, adjustment of W / L ratio of P & N channel MOS transistor for symmetrical drive output and loading consideration. Scaling of CMOS Inverter for different technologies, study of secondary effects ( temperature, power supply and process corners). Layout of CMOS Inverter, extraction of parasitics and back annotation and related modifications in circuit parameters and layout.

Current Source / Mirror: Circuit simulation of current mirror using BJT and MOS (Simple, Wilson and Widler configurations ) study and modifications to improve power and load regulation. Layout of CMOS current mirror.

8 Bit shift register cell: Building of cell Library of logic gates and flip flops and building of 8 bit shift register from the same. Optimization of the same from layout and power considerations.

Differential Amplifier: Study of specifications of differential amplifier and design considerations. Study of input loading and biasing techniques.
MTVL-201 Algorithms for VLSI Design Automation

Internal Marks: 50
External Marks: 100
Total Marks: 150

L T P
3 1 0

Logic synthesis & verification: Introduction to combinational logic synthesis, Binary decision diagram, Hardware models for High-level synthesis.

VLSI automation Algorithms Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

Placement, floor planning & pin assignment: Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.


Detailed routing: Problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

Texts / References

MTVL-202 Testing and Fault Tolerance

Internal Marks:50  L  T  P
External Marks: 100
Total Marks:150

Introduction to Testing: Role of testing VLSI circuits, VLSI trends affecting testing, Physical Faults, Stuck-at Faults, Stuck open Faults, Permanent, Intermittent and Pattern Sensitive Faults, Delay Faults.

Fault Modeling- Functional Testing, Structural Testing, Types of Fault Models, Stuck-at Faults, Bridging Faults, cross point faults, Fault Equivalence, Fault Dominance


Testability Measure – Controllability, Observability, SCOAP measures for combinational and sequential circuits.

ATPG for Combinational Circuits: Path Sensitization Methods, Roth’s D- Algorithm, PODEM Algorithm, Complexity of Sequential ATPG, Time Frame Expansion.


Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction codes, Reconfiguration Techniques, Yield Modelling Reliability.

Text Books/ References

MTVL-203 Embedded Systems

Internal Marks: 50
External Marks: 100
Total Marks: 150


- Design tradeoffs due to thermal considerations and Effects of EMI/ES etc. Software aspect of embedded systems: Challenges and issues in embedded software development, Co-design

- Embedded software development environments: Real time operating systems, Kernel architecture: Hardware, Task/process control subsystem, Device drivers, File subsystem, system calls, Embedded operating systems, Task scheduling in embedded systems: task scheduler, first in first out, shortest job first, round robin, priority based scheduling, Context switch: Task synchronization: mutex, semaphore, Timers.

- Types of embedded operating systems, Programming languages: assembly languages, high level languages for embedded systems: Embedded system development process Determine the requirements, Design the system architecture, Choose the operating system, Choose the processor, Choose the development platform, Choose programming language, Coding issues, Code optimization, Efficient input/output Testing and debugging, Verify the software on the host system, Verify the software on the embedded system.

BOOKS / REFERENCES
4. J.W. Valvano, "Embedded Microcomputer System: Real Time Interfacing"
MTVL-205 Advanced Digital Signal Processing

Internal Marks: 50
External Marks: 100
Total Marks: 150

- Design of digital filters: introduction to filter design, types of digital filters, choosing between, fir and iir filters, filter design steps, effect of finite register length in filter design, realization of iir digital filters and fir digital filter, design of iir filters from continuous time filters, design of fir filters by windowing.
- Linear estimation and predication: maximum likelihood criterion efficiency of estimator, least mean squared error criterion, recursive estimators, and linear predications.
- Multirate digital signal processing: Mathematical description of change of sampling rate, interpolation and decimation, continuous time model, direct digital domain approach, interpolation and decimation by an integer factor, single and multistage realization, applications of sub band coding.
- DSP Chips: Introduction to fixed point and floating point processors, ADSP21xx and TMS320Cxx Architecture, Memory, Addressing Modes, Interrupts, Applications. Comparison of ADSP21xx and TMS320Cxx series.

BOOKS / REFERENCES

2. Proakis, Manolakis ,” Digital Signal Processing principles, algorithms, and applications”, Prentice Hall India
4. ADSP 2181 manuals
5. Keshab K. Parhi, ” VLSI DSP Systems; Design & implementation”, WileyInterScience Publishers
MTVL-206 Semiconductor Devices

Internal Marks: 50
External Marks: 100
Total Marks: 150

Semiconductor Physics Fundamentals: Quantum Mechanics Concepts, Schrodinger wave equation, Carrier Concentration, Drift Velocity, Diffusion Transport Equation, Mobility effects, Hall Effect, Continuity Equation, Carrier Generation and Recombination, Shockley Read Hall Theory of Recombination.


Bipolar Junction Transistor: Introduction to BJT, Transistor Action, Minority carrier distribution profile, Equivalent Models -Ebers - Molls Model, Gummel Poon Model, Non-ideal effects in BJT- Early effect, High Injection etc.

MOSFET Modeling: Introduction Interior Layer, MOS Transistor Current, Energy band diagram, Threshold Voltage, Work function difference, Flat band voltage, Depletion layer thickness, Charge distribution, C-V characteristics, I-V Characteristics.

Non-ideal Effects in MOSFET: Short Channel and Narrow Width Effect, Sub-threshold Conduction, Channel length modulation, Velocity saturation, , $V_T$ roll-off, Dain Induced Barrier Lowering, Gate Induced Drain Leakage, Gate Tunneling, Punch through.


Text Books / References

MTVL-207 VLSI Interconnects

Internal Marks: 50
External Marks: 100
Total Marks: 150

Interconnects

Interconnect Parameters: Resistance, Inductance, and Capacitance, Interconnect RC Delays: Elmore Delay Calculation. Interconnect Models: The lumped RC Model, the distributed RC Model, the transmission line model. SPICE Wire Models: Distributed RC lines in SPICE, Transmission line models in SPICE.

Scaling issues in interconnects

Gate and Interconnect Delay

CMOS Repeater


Repeater Design: Driving Interconnects for Optimum speed and power

Short channel model of CMOS Repeater - Transient Analysis of an RC loaded CMOS repeater, Delay Analysis, Analytical power expressions: Dynamic power, Short circuit Power, Resistive Power Dissipation, CMOS Repeater insertion: Analytical expressions for delay and power of a repeater chain driving an RC load.

Advanced Interconnect Techniques

Reduced-swing Circuits, Current-mode Transmission Techniques

Crosstalk

Theoretical basis and circuit level modeling of crosstalk, Energy dissipation due to crosstalk: Model for energy calculation of two coupled lines. Contribution of driver and interconnect to dissipated energy, Crosstalk effects in logic VLSI circuits: Static circuits, Dynamic circuits and various remedies.

Texts / References

MTVL-208 Memory Design and Testing

Internal Marks: 50          L    T    P
External Marks: 100          3    1    0
Total Marks: 150


**Dynamic Random Access Memories (DRAMs):** DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures -BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

**Nonvolatile Memories:** Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) -Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.


**Texts / References**

MTVL-209 Low Power VLSI Design

 Internal Marks: 50
 External Marks: 100
 Total Marks: 150


Power Estimation: Simulation Power analysis- SPICE circuit simulators, Gate level logic simulation, Capacitive power estimation, Static state power, Gate level capacitance estimation, Architecture level analysis, Data correlation analysis in DSP systems. Monte Carlo simulation. Probabilistic power analysis- Random logic signals, Probability & frequency, Probabilistic power analysis techniques.

Low Power Design: Circuit level- Power consumption in circuits, Flip Flops & Latches design, High capacitance nodes, Low power digital cells library Logic level- Gate reorganization, Signal gating, Logic encoding, State machine encoding, Precomputation logic.

Low Power Architecture & Systems: Power & performance management, Switching activity reduction, Parallel architecture with voltage reduction, Flow graph transformation, Low power arithmetic components, Low power memory design.

Low Power Clock Distribution: Power dissipation in clock distribution, single driver vs distributed buffers, zero skew vs tolerable skew, chip & package co design of clock network.


Texts / References

MTVL-210 Modelling and Simulation

Internal Marks: 50
External Marks: 100
Total Marks: 150

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3 1 0

Component model for ICs: Design rule checks, timing verification worst case delay simulation, setup and hold times for clocked devices; Behaviour modeling, structural modeling, simulation with the physical model; Hardware Description Language.

Statistical: Description of data, Data-fitting methods, Regression analysis, Analysis of Variance, Goodness of fit.

Probability and Random Processes: Discrete and Continuous Distribution, Central Limit theorem, Measure of Randomness, Monte Carlo Methods.


Continuous simulation: Modelling with differential equations, Example models, Bond Graph Modelling, Population Dynamics Modelling, System dynamics.

Texts / References

MTVL-204 Lab – II

Internal Marks:100
External Marks: -
Total Marks:100

Arithmetic Unit (8-bit): Designing the Specifications and circuit of an Arithmetic Unit. Implementation of an Arithmetic Unit on FPGA.

Multiplexed Display Controller: Designing the Specifications and circuit of a Multiplexed Display Controller (MDC) Implementation of a Multiplexed Display Controller on FPGA.

Scanned Keyboard Controller: Designing the Specifications and circuit of a Scanned Keyboard Controller. Implementation of a Scanned Keyboard Controller on FPGA.

UART: Designing the Specifications and circuit of a UART. Implementation of a UART on FPGA.

CRT Controller: Designing the Specifications and circuit of a CRT Controller. Implementation of a CRT Controller on FPGA.

Filter Implementation using MAC: Designing the Specifications and circuit of a Filter Implementation using MAC. Implementation of a MAC on FPGA.

Decimal Counter and Multiplexing the Output: The purpose of this lab is to implement a decimal counter, which counts from 0 to 99. The students will be required to write a program for the AVR 8515 micro-controller.

Watchdog Timer: In this lab the students will design a hardware watchdog timer. They are ment to write a buggy program in order to test their WDT. The 8515 program should perform some computation, e.g., write 1, 2, 3 ... to the LED and at some point enter an infinite loop. During normal operation, the 8515 program must periodically (up to 254 second long cycles) write to the WDT's initial value register to avoid unnecessary resets.

AVR microcontroller UART in C: Implement AVR microcontroller UART in C

Implementation of simple calculator using AVR 8515: Implement a simple calculator using AVR 8515 microcontroller with keyboard and LCD display interface.

Analog to Digital Conversion: To implement analog to digital conversion using the ADC0804LCN 8-bit A/D converter. You will design a circuit and program the chip so that when an analog signal is given as input, the equivalent digital voltage is displayed on an LCD display.

Implementing SPI bus Using AVR 8515: To implement I2C serial communication using AVR 8515. Digital Filters with AVR Implement digital filters using low cost microcontroller from AVR series. Converting 8-bit LCD communication to 4-bit

IR Remote Control Receiver: In this lab students are required to design and implement IR remote control receiver using AVR 8515 microcontroller.

Step Motor Controller: In this lab students are meant to implement a compact size and high-speed interrupt driven step motor controller.
MTVL-304 System on Chip (SOC)

Internal Marks: 50  L   T   P
External Marks: 100  3   1   0
Total Marks: 150


Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor—memory interaction.


Verification: System Level, Block Level and Hardware/Software Co-verification, SOC components: emulation, co-simulation, Physical Verification.

Application Studies / Case Studies: AES algorithms, Image compression, VOIP, antenna for SOC etc

Text/References

1. Wayone Wolf,” Modern VLSI Design: SOC Design”
MTVL-305 RF Circuit Design

Internal Marks:50
External Marks: 100
Total Marks:150


- Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non coherent deflection. Mobile RF Communication systems and basics of Multiple Access techniques.


- Basic blocks in RF systems and their VLSI implementation: Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations.


- Power Amplifiers design. Linearization techniques, Design issues in integrated RF filters, Some discussion on available CAD tools for RF VLSI designs.

Texts / References

MTVL-306 Advanced Computer Architecture

Internal Marks: 50  
External Marks: 100  
Total Marks: 150  

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**Parallel computer models:** The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivector and SIMD computers.

**Program and network properties:** Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms.

**System Interconnect Architectures:** Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

**Advanced processors:** Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors.

**Pipelining:** Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines.

**Multiprocessor architectures:** Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization.

**Texts / References**

5. V.Rajaranam & C.S.R.Murthy, “Parallel computer” PHI.
Resistivity: Wafer mapping, two point versus four point probe, resistivity profiling (differential hall effect, spreading resistance profiling), contactless methods.

Carrier Doping: Capacitance-voltage(C-V), current-voltage(I-V), optical techniques. Contact resistance and Schottky Barriers: metal-semiconductor contacts, measurement techniques, schottky barrier height.


Texts / References

MTVL-308 Sensor Technology and MEMS

Internal Marks: 50  
External Marks: 100  
Total Marks: 150

Introduction


Micromachining techniques

Introduction to Bulk Micromachining, Isotropic and Orientation-Dependent Wet Etching, Dry Etching, Buried Oxide Process, Silicon Fusion Bonding, Sacrificial Layer Technology, Surface Micromachining using Plasma Etching, Combined IC Technology and Anisotropic Wet Etching, Processes Using Both Bulk and Surface Micromachining, Adhesion Problems in Surface Micromachining, Surface Versus Bulk Micromachining

Smart Sensors and Modeling

Introduction to Smart Sensors, Integrated Smart sensors and smart systems, MEMS and NEMS devices, Elastic structures in MEMS and NEMS, Modeling of Thermal Elastic systems, Electrostatic- elastic systems, magnetically actuated systems, Microfluidics (Membrane Pumps, Nanolithography, Nano jets)

Texts / References

1. Modeling MEMS and NEMS John A. Pelesko and David H. Bernstein Chapman & Hall/CRC
2. MEMS Fundamental Technology and Applications vikas Choudhary and Krzysztof Iniewski CRC press
7. K.D. (Guest Editor) “Integrated Sensors, Microp-actuators and micro-systems
MTVL-309 Nanoelectronics Devices

Internal Marks: 50  
External Marks: 100  
Total Marks: 150

**Introduction:** Moore’s Law and Its Significance, Size Dependent Electrical Properties in Nanomaterials: Matthiessen’s Rule, Development of Nanoelectronics; Strategies for Fabrication of Nano Devices; Development of Electronics: Semiconductor Transistors; Some Tools of Micro and Nanofabrication.


**Nanobiometrics:** Lipids as Nano-Bricks and Mortar; Self-Assembled Monolayers; The Bits that Do Things-Proteins: 3D Optical Memory, Basic Concepts on Molecular Machines and Nanoscale Motors, Nanovalves; Structure is Information-DNA: Smart Glue, Wire Template; A Biological Nanotechnology Future.

**Photonics and Solar Energy:** Properties of Light and Nanotechnology, Interaction of Light and Nanotechnology: Photon Trapping and Plasmons, Dielectric Constant and Polarization; Nanoholes and Photons; Imaging; Energy Efficient Windows and Solar Absorbers Based on Nanoparticles.

**Texts / References**

1. Nanoscience; The Science of the Small in Physics, Engineering, Chemistry, Biology and Medicine by Hans-Eckhardt Schaefer (Springer).
2. Carbon Nanotubes: Science and applications by Laurie Kelly and Meyyappan (CRS Press).
3. Handbook of Nanofabrication by Gary P. Wiederrecht (Ed.) (Elsevier)
MTVL-310 Biomedical Electronics


Electro-Physiological Measurements: Basic components of biomedical electronics system, Electrodes: Micro, Needle and Surface electrodes, Electrical activity of heart, Generation and Recording of ECG signals, ECG Waves and Time Intervals, Heart Rhythms, Heart beat morphologies, Noise and artifacts, Respiratory system, EEG, EEG Rhythms and waveforms, Recording.

Non-Electrical Parameter Measurement: Blood pressure measurement, Cardiac output, Heart Sounds, Respiratory rate, Gas volume, Flow rate, ph value, ESR, GSR, Plethysmography.

Assistive Restorative and Medical Imaging Equipments: Phonocardiography, Vectrocardiography, Defibrillators, Pacemakers, X-Ray, Ultrasonography, Computer Tomography, MRI.

Texts / References

MTVL-311 Hardware-Software Co-design

Internal Marks:50   L  T  P
External Marks: 100
Total Marks:150

Introduction: Motivation hardware & software co-design, system design consideration, research scope & overviews.

Hardware Software background: Embedded systems, models of design representation, the virtual machine hierarchy, the performance modeling, Hardware Software development.

Hardware Software co-design research: An informal view of co-design, Hardware Software tradeoffs, crosses fertilization, typical co-design process, co-design environments, limitation of existing approaches, ADEPT modeling environment.


Methodology for co-design: Amount of unification, general consideration & basic philosophies, a framework for co-design.

Unified representation for Hardware & Software: Benefits of unified representation, modeling concepts.

An abstract Hardware & Software model: Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model.

Performance evaluation: Application of the abstract Hardware & Software model, examples of performance evaluation.

Texts / References